CP9177 MULTICORE ARCHITECTURE

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UNIT I **9**

Fundamentals of SuperScalar Processor Design, Introduction to Multicore Architecture – Chip Multiprocessing, homogeneous Vs heterogeneous design - SMP – Multicore Vs Multithreading.

UNIT II **9**

Shared memory architectures– synchronization – Memory organization – Cache Memory – Cache Coherency Protocols - Design of Levels of Caches.

UNIT III **9**

Multicore programming Model – Shared memory model, message passing model, transaction model – OpenMP and MPI Programming.

UNIT IV **9**

PowerPC architecture – RISC design, PowerPC ISA, PowerPC Memory Management Power 5 Multicore architecture design, Power 6 Architecture.

UNIT V **9**

Cell Broad band engine architecture, PPE (Power Processor Element), SPE (Synergistic processing element), Cell Software Development Kit, Programming for Multicore architecture.

TOTAL: 45

TEXT BOOK:

1. Hennessey & Pateterson, “Computer Architecture A Quantitative Approach”, Harcourt Asia, Morgan Kaufmann, 1999
2. Joseph JaJa, Introduction to Parallel Algorithms, Addison-Wesley, 1992.
3. IBM Journals for Power 5, Power 6 and Cell Broadband engine architecture.

REFERENCES:

1. Kai Hwang, “Advanced Computer Architecture: Parallelism, Scalability and Programmability” McGraw-Hill, 1993
2. Richard Y. Kain, “Advanced Computer Architecture: A System Design Approach”, PHI, 1999
3. Rohit Chandra, Ramesh Menon, Leo Dagum, and David Kohr, Parallel Programming in OpenMP, Morgan Kaufmann, 2000.